**PRACTICAL 8**

**COMPUTER ORGANISATION AND ARCHITECTURE**

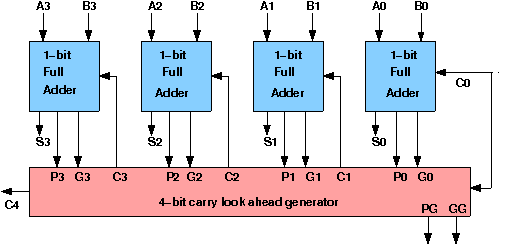
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| **BATCH: 1** | **DATE OF EXPERIMENT: 17/10/2020** |

**AIM**

**To Study & Verify Carry Look Ahead Adder**

**THEORY**

To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be Carry Propagator and Carry Generator. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry, regardless of input carry. The block diagram of a 4-bit Carry Lookahead Adder is shown here below -



The corresponding Boolean expressions are given here to construct a carry lookahead adder. In the carry-lookahead circuit we ned to generate the two signals carry propagator(P) and carry generator(G),

Pi = Ai ⊕ Bi

Gi = Ai · Bi

The output sum and carry can be expressed as

Sumi = Pi ⊕ Ci

Ci+1 = Gi + ( Pi · Ci)

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

C1 = G0 + P0 · C0

C2 = G1 + P1 · C1 = G1 + P1 · G0 + P1 · P0 · C0

C3 = G2 + P2 · C2 = G2 P2 · G1 + P2 · P1 · G0 + P2 · P1 · P0 · C0

C4 = G3 + P3 · C3 = G3 P3 · G2 P3 · P2 · G1 + P3 · P2 · P1 · G0 + P3 · P2 · P1 · P0 · C0

**SIMULATION**

